BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Charles R. Moore	:	Before the Examiner: Aimee J. Li
Serial No.: 09/737,342	:	Group Art Unit: 2183
Filed: December 15, 2000	:	
Title: DATA FLOW ORIENTED STORAGE	:	IBM Corporation Intellectual Property 11400 Burnet Road Austin, Texas 78758

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

I. REAL PARTY-IN-INTEREST

The real party in interest is International Business Machines Corporation, who is the assignee of the entire right and interest in the present Application.

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, Alexandria, VA 22313-1450, on January 19, 2005.

Serena Beller
Signature

Serena Beller
(Printed name of person certifying)

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II. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to Appellants, the Appellants' legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-50 and 55-59 are pending in the Application. Claims 1-50 and 55-59 stand rejected.

IV. STATUS OF AMENDMENTS

Amendments were made in an after Final response dated November 17, 2004. The Applicant had submitted amendments by fax to the Examiner that the Examiner stated distinguished the invention from the art cited in the Examiner's response dated October 04, 2004. The Applicant filed an after Final response after the Examiner stated the amendments would be entered. Subsequently an Advisory Action was received indicating that the amendments were not entered.

V. SUMMARY OF THE INVENTION

In one embodiment, an apparatus for managing operations in a processor, comprises:

1. A plurality of addressable registers (FIG. 14, Storage Reference Buffer (SRB) registers 0-63) each partitioned into plurality of data entry fields (FIG. 14, elements 601-607).

2. A first comparison circuit (FIG. 14, element 1512) operable to scan (FIG. 14, MUX 1511) and compare a value in a set of the data entry fields (FIG. 14, real addresses 605) to a predetermined input value (FIG. 14, input real address 1514).

3. A second comparison circuit (FIG. 14, element 1515) operable to compare a first register address (FIG. 14, element 1508) corresponding to a comparison match (FIG. 14, compare 1513 of the first comparison circuit to a second register address (FIG. 14, IN Ptr. 615 and OUT Ptr. 614)

4. A dispatch circuit (FIG. 14, element 1502) operable to dispatch data (FIG. 14, Quadword (63)) of a second data entry field (FIG. 14, element 607) of a second register (FIG. 14, determined by Address Generator 1505), corresponding to the second register address (FIG. 14, generated by Address Generator 1505 in response to element 1504), to an operation unit in response to a decode (FIG. 14, element 1503) of data in a third data entry field (FIG. 14, element 603) of the second register and a comparison match of the second comparison circuit. See Specification, page 33, lines 3-20; page 7, lines 14-20; page 7, line 21 through page 8, line 5; page 8, lines 6-14; page 8, line 23 through page 9, line 4; page 9, line 20 through page 12, line 23; and page 15, lines 4 through page 16, line 9.

In another embodiment of the invention, a data processing system comprises:

1. A central processing unit (CPU). (FIG. 13, element 1310)

2. A random access memory (RAM). (FIG. 13, element 1314)

3. A read only memory (ROM). (FIG. 13, element 1316)

4. An I/O adapter. (FIG. 13, element 1318)

5. A bus system (FIG. 13, element 1312) coupling devices internal to said CPU, said CPU comprising an apparatus for managing operations within a processor of said CPU having (Specification, page 33, lines 3-20):

a) A plurality of addressable registers (FIG. 14, SRB registers 0-63) each partitioned into plurality of data entry fields (FIG. 14, elements 601-607).

b) A first comparison circuit (FIG. 14, element 1512) operable to scan (FIG. 14, MUX 1511) and compare a value in a set of the data entry fields (FIG. 14, real addresses 605) to a predetermined input value (FIG. 14, input real address 1514).

c) A second comparison circuit (FIG. 14, element 1515) operable to compare a first register address (FIG. 14, element 1508) corresponding to a

comparison match (FIG. 14, compare 1513 of the first comparison circuit to a second register address (FIG. 14, IN Ptr. 615 and OUT Ptr. 614)

c) A dispatch circuit (FIG. 14, element 1502) operable to dispatch data (FIG. 14, Quadword (63)) of a second data entry field (FIG. 14, element 607) of a second register (FIG. 14, determined by Address Generator 1505), corresponding to the second register address (FIG. 14, generated by Address Generator 1505 in response to element 1504), to an operation unit in response to a decode (FIG. 14, element 1503) of data in a third data entry field (FIG. 14, element 603) of the second register and a comparison match of the second comparison circuit. See Specification, detailed description of FIG. 14 added to make the Specification correspond to FIG. 14. See Specification, page 7, lines 14-20; page 7, line 21 through page 8, line 5; page 8, lines 6-14; page 8, line 23 through page 9, line 4; page 9, line 20 through page 12, line 23; and page 15, lines 4 through page 16, line 9.

VI. ISSUES

1. Claims 55-59 stand rejected under *35 U.S.C. § 112*, first paragraph, as failing to comply with the enablement requirement.

2. Claims 1-12, 14-25 and 55-56 stand rejected under *35 U.S.C. § 102(b)* as being disclosed by U.S. Patent No. 5,764,946 to *Tran et al.* (hereafter "*Tran*").

3. Claim 13 stands rejected under *35 U.S.C. § 103*(a) as being unpatentable over *Tran* in view of *Jerry M. Rosenberg's* Dictionary of Computers, Information Processing & Telecommunications Second Edition© 1987 (herein referred to as "*Rosenberg*").

4. Claims 26-37 and 39-50 stand rejected under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Kenneth L. Short's* Microprocessors and Programmed Logic© 1981 (herein referred to as "*Short*").

5. Claim 38 stands rejected under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Short*.

6. Claims 57-59 stand rejected under *35 U.S.C. § 103(a)* as being unpatentable under *Tran* in view of U.S. Patent No. 5,835,962 to *Chang et al.* (hereafter "*Chang*").

VII. ARGUMENT

1. The Examiner rejected Claims 55-59 under *35 U.S.C. §112*, first paragraph, as failing to comply with the enablement requirement. The Examiner states that Claims 55-59 contain subject matter which was not described in the Specification.

Claim 55 is directed to the limitation of Claim 6 wherein the SRB comprises the plurality of addressable registers. This is completely described in the Specification. See Specification, page 2, lines 5-8.

Claim 56 is directed to a Load operation in one of the Load and Store operations which comprises the steps of 1) issuing concurrently a fetch instruction requesting a real address to a data cache and the Storage Reference Buffer (SRB), the real address corresponding to an address of multiple bytes of data, 2) scanning the addressable registers in the SRB for the real address, 3) receiving the multiple bytes of data from the SRB if the real address is available, 4) retrieving the multiple bytes of data first from the SRB if the real address is available and second from the data cache if the real address is not available in the SRB, and 5) updating a corresponding one of the addressable registers with the multiple bytes of data. This Load operation is described in the Specification relative to FIG. 7. See Specification page 21, line 16 to page 23, line 24.

Claim 57 is directed to a Store operation in one of the Load and Store operations comprising the operations of 1) issuing a real address generation

instruction, 2) looking up the real address in a table lookup buffer, 3) sending the real address to a miss resolution processor if the real address is not in the table lookup buffer, the miss resolution processor determining a translated real address, 4) sending the real address from one of the miss resolution processors and the table lookup buffer to the Storage Reference Buffer (SRB), and 5) updating corresponding data entry fields in one of the addressable registers in the SRB. This Store operation is described in the Specification relative to FIG. 8. See Specification page 20, line 1 to page 21, line 15.

Claim 58 is directed to a Store operation in one of the Load and Store operations comprising the operations of 1) issuing a real address generation instruction, 2) updating the real address in a real address field of one of the addressable registers in the SRB, 3) sending concurrently, a request for a multiple byte word with the real address to the SRB and a data cache, 4) receiving the multiple byte word from one of the addressable registers in the Storage Reference Buffer and from a data cache, 5) updating the multiple byte word from the data cache with an operand mask, 6) receiving from the first instruction unit store data operand,)7 aligning the store data operand to the multiple bytes of data, and)8 updating the multiple bytes of data with a complement of the operand mask. This Store operation is described in the Specification relative to FIG. 12. See Specification page 16, line 10 to page 17, line 2.

Claim 59 is directed to a Load operation in one of the Load and Store comprising operations of 1) issuing an address generation instruction by a first instruction unit generating a real address in a memory, 2) updating the real address in a real address field of one of the addressable registers in the SRB, 3) sending concurrently, a request for a multiple byte word with the real address to the SRB and a data cache, 4) receiving the multiple byte word from one of the addressable registers in the SRB and the data cache, 5) extracting selected bytes from the multiple byte word, 6) receiving the selected bytes by the first instruction unit, and 7) updating the multiple bytes of data with a complement of the operand mask. This Load

operation is described in the Specification relative to FIG. 11. See Specification page 14, line 22 to page 16, line 9.

The Applicants assert that the Load and Store operations are described in detail in the Specification. In the Brief Description of Drawings, FIG. 7 and FIG. 12 are identified as being directed to a Load Operation according to embodiments of the present invention and FIG. 8 and FIG. 12 are identified as being directed to a Store Operation according to embodiments of the present invention. The Detailed Description on pages 7-19 go into considerable detail with the specifics claimed in Claims 55-59. The Applicants assert that the rejections of these Claims under *35 U.S.C. §112*, first paragraph, are traversed by the Detailed Description on pages 7-19 relative to FIGS. 7, 8, 11, and 12.

2. The Examiner rejected Claims 1-12, 14-25 and 55-56 under *35 U.S.C. § 102(b)* as being disclosed by U.S. Patent No. 5,764,946 to *Tran et al.*(hereafter ("*Tran*").

Claim 1 is directed to an apparatus for managing operations in a processor comprising four interrelated elements. Element 1 is a plurality of addressable registers, wherein each register is partitioned into plurality of data entry fields. Element 2 is a first comparison circuit operable to scan and compare a value in a set of the data entry fields (within the plurality of addressable registers) to a predetermined input value. Element 3 is a second comparison circuit operable to compare a first register address, corresponding to a comparison match of said first comparison circuit, to a second register address. When the first comparison circuit finds a value in the data entry fields that matches the predetermined input value there is a comparison match and a corresponding first register address results. The second comparison circuit (Element 3) then compares the first register address to a second register address. Element 4 is a dispatch circuit operable to dispatch data, of a second data entry field of a second register corresponding to the second register address, to an operation unit in response to a decode of data in a third data entry field of the

second register and a comparison match of the second comparison circuit. The Applicants have shown that all of these elements are within the Storage Reference Buffer (SRB) of the present invention which in turn resides in the Storage Management Unit (SMU).

The Examiner argues in a conclusory statement that *Tran* teaches an apparatus of Claim 1 for managing operations of a processor in column 6, line 52 to column 7, line 14, however not detail is provided in this argument.

In the material cited, what *Tran* actually describes many elements in a block diagram of a superscalar microprocessor 200 including a branch prediction unit 220 employing a way prediction unit in accordance with the invention of *Tran*. The following are examples of the many units described by *Tran* in column 6, line 52 to column 7, line 14. As illustrated in the embodiment of FIG. 1, superscalar microprocessor 200 includes a prefetch/predecode unit 202 and a branch prediction unit 220 coupled to an instruction cache 204. Instruction alignment unit 206 is coupled between instruction cache 204 and a plurality of decode units 208A-208F (referred to collectively as decode units 208). Each decode unit 208A-208F is coupled to a respective reservation station unit 210A-210F (referred collectively as reservation stations 210), and each reservation station 210A-210F is coupled to a respective functional unit 212A-212F (referred to collectively as functional units 212). Decode units 208, reservation stations 210, and functional units 212 are further coupled to a reorder buffer 216, a register file 218 and a load/store unit 222. A data cache 224 is finally shown coupled to load/store unit 222, and an MROM unit 209 is shown coupled to instruction alignment unit 206. Generally speaking, instruction cache 204 is a high speed cache memory provided to temporarily store instructions prior to their dispatch to decode units 208. In one embodiment, instruction cache 204 is configured to cache up to 32 kilobytes of instruction code organized in lines of 16 bytes each (where each byte consists of 8 bits). During operation, instruction code is provided to instruction cache 204 by prefetching code from a main memory (not shown) through prefetch/predecode unit 202.

The Applicant respectfully asserts that the Examiner has failed to point out which of these multiplicity of units making up superscalar microprocessor 200 he considers is the apparatus of Claim 1 of the present invention. Since the apparatus of Claim 1 comprises the four elements detailed above, it is important to know which of these units the Examiner considers the apparatus of Claim 1 so that the relationship of the four elements as detailed in Claim 1 can be determined for the unit the Examiner believes teaches the invention. For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. The identical invention must be shown in as complete detail as is contained in the claim.

The Examiner states that *Tran* teaches Element 1 of Claim 1 and cites *Tran*, column 1, line 49 to column 2, line 25. For the *Tran* reference to read on Element 1 of Claim 1, the particular apparatus of *Tran* that the Examiner believes is the apparatus of Claim 1 must comprise a plurality of addressable registers, wherein each of the plurality of addressable registers is partitioned into a plurality of data entry fields. This can only be true if one of the units, cited by the Examiner as being the apparatus for managing the operations in a processor, does in fact contain the Element 1 of Claim 1. *Tran* in the recitation of column 1, line 49 to column 2, line 25 is discussing how the memory in a superscalar microprocessor are accessed. Memory does not manage any operation of a processor save for how the information stored by the memory is interpreted by another unit. The Applicants fail to see the relevance of this cited art with regards to Element 1 of Claim 1 of the present invention. Nowhere in this reference is an apparatus for managing operations of a processor mentioned, wherein the apparatus has a plurality of registers partitioned into a plurality of data entry fields. The Examiner is citing in his arguments two disjointed passages of *Tran*; a description of a block diagram of a superscalar microprocessor and a discussion of how a memory system within a superscalar microprocessor may be organized and accessed. Somehow the Examiner has determined that these disjointed passages of *Tran* teach the elements of Claim 1 directed to an apparatus for managing operations of a processor wherein the apparatus comprises a plurality of registers partitioned into data entry fields. The Applicant fails to see the connection.

The Examiner further states that *Tran* teaches Element 2 of Claim 1 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 44; and Figure 46. For these references to read on Claim 1 they must teach an apparatus for managing operations of a processor, wherein the apparatus comprises a plurality of addressable registers and a first comparison circuit, wherein each of the plurality of addressable registers is partitioned into a plurality of data entry fields and the first comparison circuit is operable to scan and compare a value in a set of the data entry fields in the plurality of addressable registers to a predetermined input value.

In the first reference, column 77, lines 33-47 *Tran* discusses operations of a line-oriented re-order buffer (LOROB). The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference column 79, lines 24-55, *Tran* discusses operations of the LOROB with the X86 instruction set. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference column 80, line 5 to column 81 line 3, *Tran* discusses the dependency checking required for store operations according to the invention of *Tran*. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference column 101, lines 45-60, *Tran* discusses the current within line dependency checking unit. The Examiner has failed to specifically point out

what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference column 102, lines 17-59, *Tran* discusses the previous lines dependency checking operation performed by the LOROB. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 38, *Tran* is showing a block diagram of the matrix dependency checking in the LOROB. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 38 was cited by the Examiner above. *Tran* is showing addresses being compared to pointers. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 39, *Tran* is showing a block diagram illustrating the dependency checking required for store operations according to his invention. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 39 was cited by the Examiner above. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 40, *Tran* is showing a block diagram illustrating the dependency checking required for load operations according to his invention. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 40 was cited by the Examiner above. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present

invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 44, *Tran* is showing a block diagram illustrating the current, within line checking unit according to his invention. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 44 was cited by the Examiner above. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 46, *Tran* is showing a block diagram illustrating the previous lines checking operation performed by the LOROB according to his invention. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 46 was cited by the Examiner above. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

The Examiner further states that *Tran* teaches Element 3 of Claim 1 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 44; and Figure 46. For these references to read on Claim 1 they must teach an apparatus for managing operations of a processor, wherein the apparatus comprises a plurality of addressable registers, a first comparison circuit and a second comparison circuit, wherein each of the plurality of addressable registers is partitioned into a plurality of data entry fields, the first comparison circuit is operable to scan and compare a value in a set of the data entry fields in the plurality of addressable registers to a predetermined input value and the second comparison circuit is operable to compare a first register address, corresponding to a comparison match of the firs comparison circuit, to a second register address. The Examiner cites the same

references of *Tran* as teaching Element 3 of Claim 1 as he cited for Element 2. Nowhere in these recitations is the invention of Claim 1 taught or suggested. Likewise, the Examiner has failed to specifically point out what he believes is Element 3 of Claim 1 of the present invention and where is the link showing the relationship of Element 3, Element 2, and Element 1 to the apparatus of Claim 1 for managing the operation of a processor in any of the cited references.

The Examiner further states that *Tran* teaches Element 4 of Claim 1 and cites *Tran*, column 106, line 35 to column 107, line 62; FIG. 48 and FIG. 49. FIG. 48 is a block diagram of a reservation station and FIG. 49 is a block diagram of the bus structure for the reservations stations according to the invention of *Tran*. In column 106, line 35 to column 107, line 62 *Tran* discusses the operation of the element of FIG. 48 and FIG. 49. Nowhere in this recitation is the invention of Claim 1 taught or suggested. Likewise, the Examiner has failed to specifically point out what he believes is Element 4 of Claim 1 of the present invention and where is the link showing the relationship of Element 4, Element 3, Element 2, and Element 1 to the apparatus of Claim 1 for managing the operation of a processor in any of the cited references.

Therefore, the Applicants assert that the Examiner has failed to make a *prima facie* case showing that *Tran* in fact teaches the invention of Claim 1 including Element 1-4 and their particular relationship recited in the limitations of Claim 1. The Examiner has found registers, comparison circuits, and dispatch circuits in the voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, the Examiner has failed to specifically point out which units of correspond to the elements of Claim 1. Therefore, the Applicants assert the rejection of Claim 1 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed.

Claim 2 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 2 adds the limitation that the operations managed by the apparatus of Claim 1 are Load and Store operations. The Examiner states the *Tran* teaches the invention of

Claim 2 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40.

Nowhere in this recitation is the invention of Claim 2 taught or suggested. Likewise, the Examiner has failed to specifically point out what he believes is the limitation Claim 2 applied to the elements of Claim 1. Therefore, the Applicants assert that the Examiner has failed to make a *prima facie* case showing that *Tran* in fact teaches the invention of Claim 2 applied to Element 1-4 and their particular relationship recited in Claim 1. The Examiner found Load and Store operations in the voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, the Examiner has failed to specifically point out which units of *Tran* correspond to the elements of Claim 1 wherein the units manage Load and Store operations. Therefore, the Applicants assert the rejection of Claim 2 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 3 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 3 adds the limitation that the predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation. The Examiner states the *Tran* teaches the invention of Claim 3 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40 which is the same reference as cited for Claim 1 and 2. The Examiner does not point out where to find the limitation of Claim 3 in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a *prima facie* case showing that *Tran* in fact teaches the invention of Claim 2 applied to Element 1-4 and their particular relationship recited in Claim 1. The Examiner found Load and Store operations in the voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, the Examiner has failed to specifically point out which units of *Tran* correspond to the elements of Claim 1

wherein the units manage Load and Store operations and the predetermined input value of Claim 1 is a real address requesting particular data corresponding to one of the Load and Store operations. Therefore, the Applicants assert the rejection of Claim 3 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 4 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 4 adds the limitation that the first comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently and in parallel. The first comparison circuit of Claim 1 is operable to scan and compare a value in a set of the data entry fields in the plurality of registers to a predetermined input value. The Examiner states the *Tran* teaches the invention of Claim 4 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40 which is the same reference as cited for Claim 1-3. The Examiner does not specifically point out the limitation of Claim 4 in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a *prima facie* case showing that *Tran* in fact teaches the invention of Claim 4 applied to Element 1-4 and their particular relationship recited in Claim 1. The Examiner found comparators in the voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, the Examiner has failed to specifically point out which units of *Tran* correspond to the elements of Claim 1 wherein the units manage Load and Store operations and the first comparator of Claim 1 is operable to scan and compare a value, in a set of said data entry fields in one of a plurality of addressable registers, each of said registers partitioned into plurality of data entry fields, to a predetermined input value and the first comparator circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently and in parallel. Therefore, the Applicants assert the rejection of Claim 4 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 5 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 5 adds the limitation that the operation unit comprises an Instruction Management Unit (IMU). The Examiner states the *Tran* teaches the invention of Claim 5 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40 which is the same reference as cited for Claim 1-4 without specifically pointing out the limitation of Claim 5 in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a *prima facie* case showing that *Tran* in fact teaches the invention of Claim 5 applied to Element 1-4 and their particular relationship recited in Claim 1. The Examiner has made the statement that the limitation of Claim 5 is in voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, the Examiner has failed to specifically point out which units of *Tran* correspond to the elements of Claim 1 wherein the management unit is an IMU. Therefore, the Applicants assert the rejection of Claim 5 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 6 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 6 adds the limitation that the operation unit of Claim 1 comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB) and the operations managed by the apparatus of Claim 1 are Load and Store operations . The Examiner states the *Tran* teaches the invention of Claim 6 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40 which is the same reference as cited for Claims 1-5 without specifically pointing out where the limitation of Claim 6 is found in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a *prima facie* case of anticipation showing that *Tran* in fact teaches the invention of Claim 6 applied to the four elements and their particular relationship recited in Claim 1. The Examiner has made the statement that the limitation of Claim 6 is in a voluminous disclosure of *Tran* describing a superscalar

microprocessor employing a way prediction unit, however, the Examiner has failed to specifically point out which units of *Tran* correspond to the elements of Claim 1 wherein the operation unit comprises a Storage Management Unit (SMU) comprising data cache memory and controller and a Storage Reference Buffer (SRB). Therefore, the Applicants assert the rejection of Claim 6 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claims 2 and 1.

Claim 7 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 7 adds the limitation that the one of the data entry fields is a Valid bit field indicating whether other data entry fields are valid. The Examiner states the *Tran* teaches the invention of Claim 7 and cites *Tran* column 123, lines 2-15. While this recitation of *Tran* mentions that the "second field of the LOROB has the linear address and store data and the associated valid bits", it does not state what the valid bit indicate and specifically doe not state that the Valid bit field indicates whether other data entry fields are valid as recited in Claim 7 of the present invention. Therefore, the Applicants assert the rejection of Claim 7 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 8 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 8 adds the limitation that one of the data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation. The Examiner states the *Tran* teaches the invention of Claim 8 and cites *Tran* column 123, lines 2-15. The Applicants have shown that *Tran* does not teach the invention of Claim 1. Therefore *Tran* does not teach Claim 8 which further limits Claim 1. Therefore, the Applicants assert the rejection of Claim 8 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the same reasons as Claim 1.

Claim 9 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 9 adds the limitation that one of the data entry fields is an instruction status field corresponding to a status of one of the Load and Store operations. The

Examiner states the *Tran* teaches the invention of Claim 8 and cites *Tran* column 123, lines 2-15. *Tran* does not mention an instruction status field in this reference and thus does not teach the limitation of Claim 9. The Applicants have shown that *Tran* does not teach the invention of Claim 1. Therefore, *Tran* does not teach Claim 9 which further limits Claim 1. Therefore, the Applicants assert the rejection of Claim 9 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the reasons above and for the same reasons as Claim 1.

Claim 10 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 10 adds the limitation that one of the data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state. The Examiner states the *Tran* teaches the invention of Claim 10 and cites *Tran* column 123, lines 2-15. In this recitation, *Tran* states that " each entry in the buffer is broken into three fields. The first field is made up of the LOROB instruction tag and the instruction type (load, store, or load-op-store)." It is clear that the first field comprises more than one bit. Claim 10 states that one of the data entry fields in the apparatus of Claim 1 is a Load/Store bit. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 1, therefore, *Tran* does not teach Claim 10 which further limits Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 10 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claim 1.

Claim 11 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 11 adds the limitation that one of the data entry fields comprises a Real Address field corresponding to a particular Real Address of memory data. The Examiner states the *Tran* teaches the invention of Claim 12 and cites *Tran* column 123, lines 2-15. In this recitation, "the first field is made up of the LOROB instruction tag and the instruction type (load, store, or load-op-store). The second field has the linear address and store data and the associated valid bits, the update

source being the functional units. The third field is made up of some control information (e.g., M bit indicating that this entry missed the data cache on a prior access, D bit indicating that the load in the entry is dependent on a store in the buffer), the update source being the load-store section itself." All of the fields in the LOROB of *Tran* are accounted for and none of them is described as comprising a Real Address field corresponding to a particular Real Address of memory data as recited in Claim 11 of the present invention. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 1, therefore, *Tran* does not teach Claim 11 which further limits Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 11 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claim 1.

Claim 12 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 12 adds the limitation that one of the data entry fields one of said data entry fields is a Quadword field comprising multiple bytes of data. The Examiner states the *Tran* teaches the invention of Claim 12 and cites *Tran* column 123, lines 2-15. In this recitation, "the first field is made up of the LOROB instruction tag and the instruction type (load, store, or load-op-store). The second field has the linear address and store data and the associated valid bits, the update source being the functional units. The third field is made up of some control information (e.g., M bit indicating that this entry missed the data cache on a prior access, D bit indicating that the load in the entry is dependent on a store in the buffer), the update source being the load-store section itself." All of the fields in the LOROB of *Tran* are accounted for and none of them is described as is a Quadword field comprising multiple bytes of as recited in Claim 12 of the present invention. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 1, therefore, *Tran* does not teach Claim 12 which further limits Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 12 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claim 1.

Claim 14 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 14 adds the limitation that the operation unit is a pipeline execution unit operating concurrently on a plurality of the data entry fields. The Examiner states the *Tran* teaches the invention of Claim 14 and cites *Tran* column 10, lines 17-25 and FIG. 1. FIG. 1 of *Tran* is a block diagram of a superscalar microprocessor employing a branch prediction unit in accordance with the invention of *Tran*. See *Tran*, column 4, lines 32-34. Since a superscalar microprocessor is a CPU architecture that allows more than one instruction to be executed in one clock cycle, one of ordinary skill in the art would assume that *Tran* in FIG. 1 is showing the execution of multiple branch instructions in parallel. The Examiner has stated in his rejection of Claims 8-12 that he believes the data entry fields of Claim 1 are disclosed relative to the LOROB. FIG. 1 of *Tran* is not illustrating a pipeline execution unit operating concurrently on a plurality of the data entry fields of the LOROB of *Tran*. Therefore, the Applicants do not see the connection between the cited reference of *Tran* and Claim 14 of the present invention. The limitation of Claim 14 is relative to a specific apparatus as recited in Claim 1. FIG. 1 and column 10, lines 15-55 are describing branch prediction operations and functional units relative the superscalar microprocessor of *Tran*. The Applicants, respectfully assert that the Examiner must be consistent in his argument that a reference is disclosing inventive elements. The Examiner cannot assert that the data entry fields of Claim 1 are in the LOROB of *Tran* in one instance and then assert that parallel operations on branch instructions (FIG. 1 of *Tran*) teach a pipeline execution unit operating concurrently on a plurality of the same data entry fields (in LOROB). The Applicants have shown the data entry fields of the LOROB of *Tran* are not the data entry fields of Claim 1 of the present invention. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 1, therefore, *Tran* does not teach Claim 14 which further limits Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 14 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claim 1.

Claim 15 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 15 adds the limitation that the addressable registers are addressed using a

plurality of address pointers. The Examiner states the *Tran* teaches the invention of Claim 15 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40, which is the same reference as cited for Claims 1-5, without specifically pointing out where the limitation of Claim 15 is found in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a *prima facie* case showing that *Tran* in fact teaches the invention of Claim 15 applied to Element 1-4 and their particular relationship recited in Claim 1. Therefore, the Applicants assert the rejection of Claim 15 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 16 depends from Claim 6 where the Storage Reference Buffer (SRB) is first introduced. Claim 16 depends from Claim 6 and contains all the limitations of Claim 6. Claim 16 adds the limitation that the addressable registers of Claim 1 are configured as the SRB. The Examiner states the *Tran* teaches the invention of Claim 16 and cites *Tran* column 10, line 66 to column 11, line 15, column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; Figure 1, Figure 38; Figure 39; and Figure 40 without specifically pointing out where the limitation of Claim 16 is found in these multiple references of *Tran*. The Examiner does not specifically point out the limitation of Claim 16 in these multiple references of *Tran*, therefore, the Applicants assert that the Examiner has failed to make a *prima facie* case showing that *Tran* in fact teaches the invention of Claim 16 applied to the four elements and their particular relationship recited in Claims 1 and 6. Therefore, the Applicants assert the rejection of Claim 16 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claims 1 and 6.

Claim 17 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 17 adds the limitation that one of the address pointers is a third pointer pointing to one of the addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register

address of a current Load operation. The Examiner states that *Tran* teaches the invention of Claim 17 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In this recitation *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein one of the address pointers is a third pointer pointing to one of the addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation. as recited in Claim 17. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 17 which further limits Claim 15. Therefore, the Applicants respectfully assert that the rejection of Claim 17 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 18 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 18 adds the limitation that the address pointers comprise a fourth and fifth pointer defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage. The Examiner states that *Tran* teaches the invention of Claim 18 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the address pointers comprise a fourth and fifth pointer defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage as recited in Claim 18. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 18 which further limits Claim 15. Therefore, the Applicants respectfully

assert that the rejection of Claim 18 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 19 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 19 adds the limitation that the second register address is selected from registers addresses which fall within a window of register addresses defined by the address pointers. The Examiner states that *Tran* teaches the invention of Claim 19 and cites *Tran* column 70, lines 7-44; column 81, lines 1-3 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the second register address is selected from registers addresses which fall within a window of register addresses defined by the address pointers as recited in Claim 19. In column 80, lines 1-3, *Tran* discloses that (sic) "the LOROB must partially retire the line until all entries with the load-match bits. The WRPTR signal indicates the load instructions can be executed." Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the second register address is selected from registers addresses which fall within a window of register addresses defined by the address pointers as recited in Claim 19. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 19 which further limits Claim 15. Therefore, the Applicants respectfully assert that the rejection of Claim 19 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 20 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 20 adds the limitation that one of the address pointers is a first pointer pointing to an IN register address of a first available register into which data may be added. The Examiner states that *Tran* teaches the invention of Claim 20 and cites

Tran column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein one of the address pointers is a first pointer pointing to an IN register address of a first available register into which data may be added as recited in Claim 20 . Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 20 which further limits Claim 15. Therefore, the Applicants respectfully assert that the rejection of Claim 20 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 21 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 21 adds the limitation that one of said address pointers is a second pointer pointing to an OUT register address of a first available register from which register data may be retired. The Examiner states that *Tran* teaches the invention of Claim 21 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein one of said address pointers is a second pointer pointing to an OUT register address of a first available register from which register data may be retired as recited in Claim 21. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 21 which further limits Claim 15. Therefore, the Applicants respectfully assert that the rejection of Claim 21 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 22 is dependent from Claim 16 and contains all the limitations of Claim 15. Claim 22 adds the limitation that the data entry fields, added to the SRB after a mis-predicted branch instruction occurs in said processor, are retired and the first pointer is indexed to a first register address of a register with added register data entry bits which were added immediately prior to the mis-predicted branch instruction. The Examiner states that *Tran* teaches the invention of Claim 22 and cites *Tran* column 82, lines 63 to column 83, line 22. In column 82, lines 63 to column 83, line 22, *Tran* discloses that mis-prediction of branches are handled by the LOROB. *Tran* then describes what happens in his LOROB in response to the two types of branches. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the data entry fields, added to the SRB after a mis-predicted branch instruction occurs in said processor, are retired and the first pointer is indexed to a first register address of a register with added register data entry bits which were added immediately prior to the mis-predicted branch instruction as recited in Claim 22. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 16, therefore, *Tran* does not teach Claim 22 which further limits Claim 16. Therefore, the Applicants respectfully assert that the rejection of Claim 22 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 16.

Claim 23 is dependent from Claim 19 and contains all the limitations of Claim 19. Claim 23 adds the limitation that the window of register addresses defines active Load and Store operations. The Examiner states that *Tran* teaches the invention of Claim 23 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the second register address is selected from registers addresses which fall within a

window of register addresses defined by the address pointers and the window of register addresses defines active Load and Store operations as recited in Claim 23. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 19, therefore, *Tran* does not teach Claim 23 which further limits Claim 19. Therefore, the Applicants respectfully assert that the rejection of Claim 23 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 19.

Claim 24 is dependent from Claim 20 and contains all the limitations of Claim 20. Claim 24 adds the limitation that the first pointer is indexed by one when the register data has been added and the first pointer has a minimum and a maximum value wherein a decrement down from a minimum value results in the maximum value and an increment up from the maximum value results in the minimum value. The Examiner states that *Tran* teaches the invention of Claim 24 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the first pointer is indexed by one when the register data has been added and the first pointer has a minimum and a maximum value wherein a decrement down from a minimum value results in the maximum value and an increment up from the maximum value results in the minimum value as recited in Claim 24. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 20, therefore, *Tran* does not teach Claim 24 which further limits Claim 20. Therefore, the Applicants respectfully assert that the rejection of Claim 24 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 20.

Claim 25 is dependent from Claim 21 and contains all the limitations of Claim 21 . Claim 25 adds the limitation that the second pointer is indexed by one when

register entry bits have been deleted and the second pointer has a minimum and a maximum value wherein a decrement down from the minimum value results in the maximum value and an increment up from the maximum value results in the minimum value. The Examiner states that *Tran* teaches the invention of Claim 25 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the second pointer is indexed by one when register entry bits have been deleted and the second pointer has a minimum and a maximum value wherein a decrement down from the minimum value results in the maximum value and an increment up from the maximum value results in the minimum value as recited in Claim 24. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 21, therefore, *Tran* does not teach Claim 24 which further limits Claim 21 . Therefore, the Applicants respectfully assert that the rejection of Claim 25 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 21.

Claim 55 is dependent from Claim 6 and contains all the limitations of Claim 6. Claim 6 adds the limitation that the operation unit of Claim 2 contains an SRB. Claim 55 adds the limitation that the Storage Reference Buffer (SRB) of Claim 6 contains the plurality of registers recited in Claim 1 and thus dependent Claim 6. The Examiner states that *Tran* teaches Claim 55 and cites *Tran* column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40. In column 10, line 66 to column 11, line 15, *Tran* describes data cache 224 and some general functions of load/store unit 222. *Tran* also states that the load/store unit has a load/store buffer with 16 storage locations for address and data information for pending load and store operations. Claim 55 is recites an

apparatus for managing Load and Store operations for a processor wherein the apparatus has the plurality of registers in an Storage Reference Buffer (SRB)and the other elements with the particular functionality described in Claim 1. The Applicants have shown that *Tran* does not teach or suggest the invention of Claim 2. The recitations of *Tran* cited by the Examiner only shows that *Tran* discloses a load/store buffer that has a plurality of addressable registers , however, *Tran* does not teach or suggest the particular limitations of Claim 55. Therefore, the Applicants respectfully assert that the rejection of Claim 55 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 2 and 6.

Claim 56 is dependent from Claim 55 and contains all the limitations of Claim 55. Claim 56 adds specific limitations to the Load operations when the operations managed by the apparatus of Claim 1 are Load and Store operations and the operation unit contains the SRB of Claim 55. Further Claim 56 adds the limitations of specifically how the Load operation functions with the SRB of Claim 55. Claim 56 defines the particular Load operation for the SRB of Claim 55 as comprising all of the steps of:

a) issuing concurrently a fetch instruction requesting a real address to a data cache and the Storage Reference Buffer (SRB) (operation unit of Claim 55), the real address corresponding to an address of multiple bytes of data.

The Applicants have shown that *Tran* does not teach or suggest the particular SRB of Claim 55. The operation is directed specifically to the SRB of Claim 55 with the functionality described in Claim 1. The Examiner states that *Tran* teaches this issuing step of Claim 56 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40. The Examiner has failed to specifically point out which element of *Tran* are the elements of Claim 1 with the limitations further described in dependent Claims 2, 6 and 55. The Examiner must point out which apparatus (of Tran) manages Load/Store **operations using the plurality of**

registers in the SRB and which elements are the elements of Claim 1 with the particular stated functionality.

b) scanning the addressable registers in the SRB for the real address.

The Applicants have shown that *Tran* does not teach or suggest scanning as recited in Claim 1. The scanning operation has been explained in detail in the Specification. The element that performs scanning is recited in Claim 1. The Examiner states the *Tran* teaches this scanning step of Claim 56 and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40. The Examiner has not specifically pointed out what element of *Tran* does the specific scanning step of Claim 56 or what unit is the SRB of Claim 56 and thus fails to make a *prima facie* case of anticipation.

c) receiving the multiple bytes of data from the SRB if the real address is available.

The Examiner states that *Tran* teaches this receiving step of the Load operation of Claim 56 and again cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40. The Examiner has not specifically pointed out the receiving step of Claim 56 or what unit is the SRB of Claim 56 and thus fails to make a *prima facie* case of obviousness.

d) retrieving the multiple bytes of data first from the SRB if the real address is available and second from the data cache if the real address is not available in the SRB.

The Examiner states the *Tran* teaches this retrieving step of the Load operation of Claim 56 and again cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40. The Examiner has not specifically pointed out the retrieving step of Claim 56 or what unit is the SRB of Claim 56 and thus fails to make a *prima facie* case of anticipation.

e) updating a corresponding one of the addressable registers (of the SRB of Claim 55) with the multiple bytes of data.

Again, the Examiner states the *Tran* teaches this updating step of the Load operation of Claim 56 and again cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40. The Examiner has not specifically pointed out the retrieving step of Claim 56 or what unit is the SRB of Claim 56 and thus fails to make a *prima facie* case of anticipation. Therefore, the Applicants respectfully assert that the rejection of Claim 56 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 2, 6, and 55.

3. The Examiner rejected Claim 13 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Jerry M. Rosenberg's* Dictionary of Computers, Information Processing &Telecommunications Second Edition © 1987 (herein referred to as *Rosenberg*).

Claim 13 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 13 adds the limitation that one of the data entry fields is an Operand Mask field defining selected bytes of data within a selected one of the data entry fields. The Examiner states that *Tran* does not explicitly teach the invention of Claim 13. However, the Examiner states that *Tran* does teach miscellaneous control fields. The Applicants assert that it is not enough for *Tran* to teach miscellaneous control fields for *Tran* to read on Claim 13 of the present invention. Claim 13 only adds a limitation to the apparatus of Claim 1. The Applicants have shown that *Tran* does not teach or disclose an apparatus comprising four elements for managing operations in a processor with the relationship described in Claim 1, where in addition, one of the data entry fields is an Operand Mask field defining selected bytes of data within a selected one of the data entry fields. Claim 1 is not reciting just any mask field (*Rosenberg* is simply presenting the definition of a mask field), rather Claim 1 is

directed to particular data entry fields in the registers of the apparatus of Claim 1. An "operand" is the part of a machine instruction that references data. For example, in the instruction, "ADD A to B", A and B are the operands (nouns), and ADD is the operation code (verb). Therefore the Operand Mask field of Claim 13 refers to a particular mask that is one of the plurality of data entry fields in each of the plurality of addressable registers in the apparatus of Claim 1. In turn, the Operand Mask field of Claim 13 defines selected bytes of data within a selected one of the data entry fields of the addressable registers. *Rosenberg* adds nothing to the disclosure of *Tran* because *Tran* does not disclose that his control information is used to define selected bytes of data within a selected one of data entry fields of addressable registers in the apparatus of Claim 1. One of ordinary skill in the art would not look to *Rosenberg* to determine the function to apply to the control bits of *Tran*. The invention of Claim 13 could only be arrived at by combining *Tran* and *Rosenberg* using hindsight in view of the present invention. Simply knowing that *Tran* uses control bits and having *Rosenberg*'s definition of a mask field does not lead one of ordinary skill in the art to the invention of Claim 13. Therefore, the Applicants respectfully assert that the rejection of Claim 13 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Rosenberg* is traversed for the above arguments and for the same reasons as Claims 1.

4. The Examiner rejected Claims 26-37 and 39-50 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Kenneth L Short's* Microprocessors and Programmed Logic © 1981 (herein referred to as *Short*).

Claim 26 is an independent claim directed to a data processing system that comprises a number of units including a processor that has the apparatus with the limitations of Claim 1. The Applicants have shown that *Tran* does not teach or disclose the apparatus of Claim 1. The Examiner states that *Tran* teaches a data processing system comprising a CPU wherein the CPU includes the apparatus of Claim 1. *Tran* teaches a superscalar microprocessor, the Applicants have shown that *Tran* does not teach or disclose the apparatus of Claim 1 within this superscalar

microprocessor, hence *Tran* does not teach the invention of Claim 26. The Examiner states the *Tran* does not teach a microprocessor comprising RAM, ROM, an I/O adapter, and a bus system coupling devices internal to the CPU. However, the Examiner states that *Short* teaches a microprocessor comprising RAM, ROM, an I/O adapter, and a bus system coupling devices internal to the CPU. What is important is that *Short* does not teach or suggest a CPU the includes the apparatus of Claim 1. In fact, *Short* does not teach RAM and does not teach a bus system coupling devices internal to the CPU. *Short* is only used to show the general architecture of a microprocessor not included in the microprocessor of *Tran*. *Short* adds no teaching or suggestion that his defined microprocessor has a CPU with the apparatus of Claim 1. The Applicants respectfully assert that *Tran* and *Short* singly or in combination, do not teach or suggest the apparatus of Claim 1. Therefore, the Applicants assert that the rejection of Claim 26 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Rosenberg* is traversed for the above arguments and for the same reasons as Claim 1.

Claims 27-37 and 39-50 add the same limitations to Claim 26 and intervening claims as Claims 2-12 and 14-25 add to Claim 1 and intervening claims. The Examiner has rejected Claims 27-37 and 39-50 for the same reasons he has rejected Claims 2-12 and 14-25 with the exception that he relies on the teachings of *Short* for the units in the CPU of Claim 26 not disclosed by *Tran*. The Applicants have shown that *Short* adds nothing to the teachings of *Tran* relative to the apparatus of Claim 1. Therefore the Applicants respectfully assert that the rejections of Claims 27-37 and 39-50 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Rosenberg* are traversed for the above arguments and for the same reasons as Claims 2-12 and 14-25.

5. The Examiner rejected Claims 38 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Short* and further in view of *Rosenberg*. Claim 38 is dependent from Claim 26 and contains all the limitations of Claim 26. Claim 13 adds the limitation that one of the data entry fields is an Operand Mask field defining

selected bytes of data within a selected one of the data entry fields of the apparatus in the data processing system of Claim 26. The Examiner states that *Tran* has not explicitly taught that one of the data entry fields is an Operand Mask field defining selected bytes of data within a selected one of the data entry fields. The Applicants have shown relative to Claim 13 that *Tran* in view of *Rosenberg* does not teach the apparatus of Claim 13. Claim 38 recites a data processing system including the apparatus of Claim 13 and the Examiner relies on *Short* to simply teach the elements of the data processing system of Claim 38 the Examiner deems are not taught by Tran. *Short* adds no teaching relative to the apparatus of Claim 26 with limitation added by Claim 38. Therefore, the Applicants respectfully assert that the rejection of Claim 38 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Rosenberg* and further in view of *Short* is traversed for the above arguments and for the same reasons as Claims 13 and 26.

6. The Examiner rejected Claims 57-59 under *35 U.S.C. § 103(a)* as being unpatentable under *Tran* in view of U.S. Patent 5, 835,962 to *Chang et al.*, hereafter ("*Chang*").

The Examiner states that *Tran* has taught updating corresponding data entry fields in one of the addressable registers in the SRB but has not taught the Store operation of Claim 57. The Applicant has shown that *Tran* does not teach or suggest the SRB of Claim 6 from which Claim 57 indirectly depends. The Examiner states that *Tran* does not teach the Store operation of Claim 57. The Examiner does state that *Chang* teaches the Store operation of Claim 57 and cites Chang, column 2, line 66 to column 2, line 28.

Claim 57 is dependent from Claim 55 and contains all the limitations of Claim 55. Claim 57 adds the limitation that the Store operation in one of the Load and Store operations of Claim 2 all the steps of:

a) issuing a real address generation instruction. Nowhere in the recitation of *Chang* does *Chang* teach or suggest issuing a real address generation instruction.

b) looking up the real address in a table lookup buffer. *Chang* recites a TLB that stores a virtual address, a real address, and various status bits.

c) sending the real address to a miss resolution processor if the real address is not in the table lookup buffer, the miss resolution processor determining a Translated real address. *Chang* does not teach or suggest a miss resolution processor or sending the real address to a miss resolution processor.

d) sending the real address from one of the miss resolution processors and the table lookup buffer to the SRB. *Chang* does not teach or suggest the SRB of Claim 55 with the apparatus of Claim 1.

e) updating corresponding data entry fields in one of the addressable registers in the SRB. The Applicants have shown that *Tran* does not teach or suggest the SRB of claim 55 having the addressable registers of the apparatus of Claim 1. Therefore, *Tran* cannot teach or suggest updating corresponding data entry fields in one of the addressable registers in the SRB. *Chang* adds no teaching or suggesting relative to the SRB of Claim 55.

The Examiner has failed to show that *Tran* in view of *Chang* singly or in combination teach or suggest the particular Store operation recited in Claim 57 of the present invention. Therefore, the Applicants respectfully assert that the rejection of Claim 57 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Chang* is traversed for the above arguments and for the same reasons as Claims 55 and 6.

Claim 58 depends from Claim 55 and contains all the limitations of Claim 55. Claim 58 adds the limitation that the Store operation in one of the Load and Store operations of Claim 2 comprises all the steps of:

a) issuing an address generation instruction by a first instruction unit generating a real address in memory.

b) updating the real address in a real address field of one of the addressable registers in the SRB.

c) sending concurrently, a request for a multiple byte word with the real address to the SRB and a data cache.

d) receiving the multiple byte word from one of the addressable registers in the Storage Reference Buffer and from a data cache.

e) updating the multiple byte word from the data cache with an operand mask.

f) receiving from the first instruction unit store data operand.

g) aligning the store data operand to the multiple bytes of data.

h) updating the multiple bytes of data with a complement of the operand mask.

The Examiner rejected Claim 58 reciting *Tran* as teaching steps c) through h) and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40. The Applicants have shown that these recitations of *Tran* do not teach or suggest the processes of steps c) through h) when applied to the apparatus of Claim 1 where operations are Load and Store operations and the plurality of addressable registers are in the SRB of Claim 55. The Examiner states that *Chang* teaches steps a) and b) of Claim 58. Again the Applicants have shown that Change does not teach or suggest the processes of steps a) and b) when applied to when applied to the apparatus of Claim 1 where operations are Load and Store operations and the plurality of addressable registers are in the SRB of Claim 55. Therefore, the Applicants respectfully assert that the rejection of Claim 58 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Chang* is traversed for the above arguments and for the same reasons as Claims 55 and 6.

Claim 59 depends from Claim 55 and contains all the limitations of Claim 55. Claim 59 adds the limitation that the Load operation in one of the Load and Store operations of Claim 2 comprises all the steps of:

a) issuing an address generation instruction by a first instruction unit generating a real address in a memory;

b) updating the real address in a real address field of one of the addressable registers in the SRB;

c) sending concurrently, a request for a multiple byte word with the real address to the SRB and a data cache;

d) receiving the multiple byte word from one of the addressable registers in the SRB and the data cache;

e) extracting selected bytes from the multiple byte word;

f) receiving the selected bytes by the first instruction unit; and

g) updating the multiple bytes of data with a complement of the operand mask.

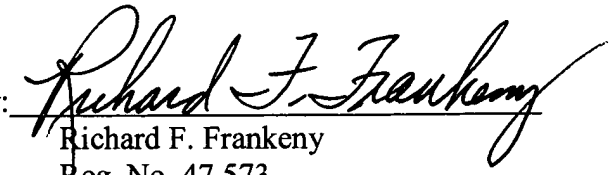
The Examiner rejected Claim 59 reciting *Tran* as teaching steps c) through h) and cites *Tran* column 77, lines 33-47; column 79, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40. The Applicants have shown that these recitations of *Tran* do not teach or suggest the processes of steps c) through h) when applied to the apparatus of Claim 1 where operations are Load and Store operations and the plurality of addressable registers are in the SRB of Claim 55. The Examiner states that *Chang* teaches steps a) and b) of Claim 59. Again the Applicants have shown that *Chang* does not teach or suggest the processes of steps a) and b) when applied to when applied to the apparatus of Claim 1 where operations are Load and Store operations and the plurality of addressable registers are in the SRB of Claim 55. Therefore, the Applicants

respectfully assert that the rejection of Claim 59 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Chang* is traversed for the above arguments and for the same reasons as Claims 55 and 56.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Patent Agent and Attorney for Appellants

By: 

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APPENDIX

1. An apparatus for managing operations in a processor, said apparatus comprising:

a plurality of addressable registers, each of said registers partitioned into plurality of data entry fields;

a first comparison circuit, said first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value;

a second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address; and

a dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit.

2. The apparatus of claim 1, wherein said operations are Load and Store operations within said processor.

3. The apparatus of claim 1, wherein said predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation.

4. The apparatus of claim 1, wherein said first comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently in parallel.

5. The apparatus of claim 1, wherein said operation unit comprises an Instruction Management Unit (IMU).

6. The apparatus of claim 2, wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB).

7. The apparatus of claim 1, wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid.

8. The apparatus of claim 1, wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation.

9. The apparatus of claim 1, wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations.

10. The apparatus of claim 1, wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state.

11. The apparatus of claim of claim 1, wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data.

12. The apparatus of claim 1, wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data.

13. The apparatus of claim 1, wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields.

14. The apparatus of claim 1, wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields.

15. The apparatus of claim 1, wherein said addressable registers are addressed using a plurality of address pointers.

16. The apparatus of claim 6 wherein said addressable registers are configured as said Storage Reference Buffer (SRB).

17. The apparatus of claim 15, wherein one of said address pointers is a third pointer, said third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation.

18. The apparatus of claim 15, wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage.

19. The apparatus of claim 15, wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers.

20. The apparatus of claim 15, wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added.

21. The apparatus of claim 15, wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired.

22. The apparatus of claim 16, wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were added immediately prior to said mis-predicted branch instruction.

23. The apparatus of claim 19, wherein said window of register addresses defines active Load and Store operations.

24. The apparatus of claim 20, wherein said first pointer is indexed by one when said register data has been added, said first pointer having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

25. The apparatus of claim 21, wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

26. A data processing system, comprising:

a central processing unit (CPU);

random access memory (RAM);

read only memory (ROM);

an I/O adapter; and

a bus system coupling devices internal to said CPU, said CPU comprising an apparatus for managing operations within a processor of said CPU, said apparatus comprising:

a plurality of addressable registers, each of said addressable registers partitioned into plurality of data entry fields;

a first comparison circuit, said first comparison circuit operable to scan and compare a predetermined input value to a value from a first data entry field selected from each of said addressable registers;

a second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address; and

a dispatch circuit operable to dispatch data in a second data entry field of a second register to an operation unit, said second register corresponding to said second register address in response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit.

27. The data processing system of claim 26, wherein said operations are Load and Store operations within said processor.

28. The data processing system of claim 26, wherein said predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation.

29. The data processing system of claim 26, wherein said first [[scan]] comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently in parallel.

30. The data processing system of claim 26, wherein said operation unit comprises an Instruction Management Unit (IMU).

31. The data processing system of claim 27, wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB).

32. The data processing system of claim 26, wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid.

33. The data processing system of claim 26, wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation.

34. The data processing system of claim 26, wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations.

35. The data processing system of claim 26, wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state.

36. The data processing system of claim of claim 26, wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data.

37. The data processing system of claim 26, wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data.

38. The data processing system of claim 26, wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields.

39. The data processing system of claim 26, wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields.

40. The data processing system of claim 26, wherein said addressable registers are addressed using a plurality of address pointers.

41. The data processing system of claim 31 wherein said addressable registers are configured as said Storage Reference Buffer (SRB).

42. (original) The data processing system of claim 40, wherein one of said address pointers is a third pointer, said third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation.

43. The data processing system of claim 40, wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window

of register addresses from which a Load operation may be satisfied without having to access other memory storage.

44. The data processing system of claim 40, wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers.

45. The data processing system of claim 40, wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added.

46. The data processing system of claim 40, wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired.

47. The data processing system of claim 41, wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were added immediately prior to said mis-predicted branch instruction.

48. The data processing system of claim 44, wherein said window of register addresses defines active Load and Store operations.

49. The data processing system of claim 45, wherein said first pointer is indexed by one when said register data has been added, said first pointer having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

50. The data processing system of claim 46, wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum

value results in said maximum value and an increment up from said maximum value results in said minimum value.

Claims 51-54 (canceled)

55. The apparatus of claim 6, wherein the SRB comprises the plurality of addressable registers.

56. The apparatus of claim 55, wherein a Load operation in one of the Load and Store operations comprises:

issuing concurrently a fetch instruction requesting a real address to a data cache and the Storage Reference Buffer (SRB), the real address corresponding to an address of multiple bytes of data;

scanning the addressable registers in the SRB for the real address;

receiving the multiple bytes of data from the SRB if the real address is available;

retrieving the multiple bytes of data first from the SRB if the real address is available and second from the data cache if the real address is not available in the SRB; and

updating a corresponding one of the addressable registers with the multiple bytes of data.

57. The apparatus of claim 55, wherein a Store operation in one of the Load and Store operations comprises:

issuing a real address generation instruction;

looking up the real address in a table lookup buffer;

sending the real address to a miss resolution processor if the real address is not in the table lookup buffer, the miss resolution processor determining a Translated real address;

sending the real address from one of the miss resolution processors and the table lookup buffer to the SRB; and

updating corresponding data entry fields in one of the addressable registers in the SRB.

58. The apparatus of claim 55, wherein a Store operation in one of the Load and Store operations comprises:

issuing an address generation instruction by a first instruction unit generating a real address in memory;

updating the real address in a real address field of one of the addressable registers in the SRB;

sending concurrently, a request for a multiple byte word with the real address to the SRB and a data cache;

receiving the multiple byte word from one of the addressable registers in the Storage Reference Buffer and from a data cache;

updating the multiple byte word from the data cache with an operand mask;

receiving from the first instruction unit store data operand;

aligning the store data operand to the multiple bytes of data; and

updating the multiple bytes of data with a complement of the operand mask.

59. The apparatus of claim 55, wherein a Load operation in one of the Load and Store operations comprises:

issuing an address generation instruction by a first instruction unit generating a real address in a memory;

updating the real address in a real address field of one of the addressable registers in the SRB;

sending concurrently, a request for a multiple byte word with the real address to the SRB and a data cache;

receiving the multiple byte word from one of the addressable registers in the SRB and the data cache;

extracting selected bytes from the multiple byte word;

receiving the selected bytes by the first instruction unit; and

updating the multiple bytes of data with a complement of the operand mask.